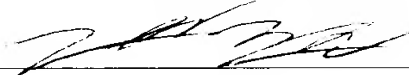


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**METHOD OF MAKING A PLANARIZED SEMICONDUCTOR STRUCTURE**

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## **BACKGROUND OF THE INVENTION**

### 1. Field of the Invention

5           This invention relates to semiconductor device manufacturing, and more particularly, to an improved method for processing a semiconductor topography.

### 2. Description of the Related Art

10           The following descriptions and examples are not admitted to be prior art by virtue of their inclusion within this section.

          Forming substantially planar surfaces during the processing of a semiconductor topography may involve numerous fabrication steps. For example, a layer may be formed  
15       across a previously patterned layer of a semiconductor topography using a process such as chemical vapor deposition ("CVD"). Elevational disparities of the deposited layer may be reduced by planarizing the layer using a process such as chemical mechanical polishing ("CMP"). Alternatively, an opening or a trench may be formed within a semiconductor topography and subsequently filled with a layer of trench fill material. In  
20       this manner, the layer of trench fill material may be formed within the opening and on an upper surface of the semiconductor surface. The layer of trench fill material may then be planarized such that an upper surface of the structure within the trench may be substantially planar with an upper surface of the semiconductor topography.

25           Substantially planar surfaces within a semiconductor topography may play an important role in the functionality of a semiconductor device. For example, step coverage problems may arise when a dielectric, conductive, or semiconductive material is deposited over a surface having raised and recessed regions. Step coverage is defined as a measure of how well a film conforms over an underlying step and is expressed by the  
30       ratio of the minimum thickness of a film as it crosses a step to the nominal thickness of

the film over horizontal regions. Furthermore, substantially planar surfaces may become increasingly important as the feature sizes of semiconductor devices are reduced, since the depth of focus required to pattern an upper surface of a topography may increase with reductions in feature size. If a topography is nonplanar, the patterned image may be  
5 distorted and the intended structure may not be formed to the specifications of the device. Furthermore, correctly patterning layers upon a surface containing fluctuations in elevation may be difficult using optical lithography. The depth-of-focus of the lithography alignment system may vary depending upon whether the resist resides in an elevational "hill" or "valley" area.

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As mentioned above, CMP is a technique that may be employed to planarize or remove the elevational fluctuations in the surface of a semiconductor topography. A conventional CMP process may involve placing a semiconductor wafer face-down on a polishing pad which lies on or is attached to a table or platen. During the CMP process,  
15 the polishing pad and/or the semiconductor wafer may be set into motion as the wafer is forced against the pad. For example, the polishing pad and the wafer may be placed on rotatable tables such that the wafer and the polishing pad may be rotated relative to each other. Alternatively, the wafer may be rotated relative to a fixed pad or vice versa. In another embodiment, the polishing pad may be a belt, which traverses against a fixed or  
20 rotating wafer. An abrasive, fluid-based chemical suspension, often referred to as a "slurry," may be deposited onto the surface of the polishing pad. The slurry fills the space between the polishing pad and the wafer surface such that a chemical in the slurry may react with the surface material being polished. The rotational movement of the polishing pad relative to the wafer causes abrasive particles entrained within the slurry to  
25 physically strip the reacted surface material from the wafer. Therefore, the process may employ a combination of chemical stripping and mechanical polishing to form a planarized surface.

Unfortunately, a CMP process may not form a substantially planar surface across the entire semiconductor topography. For instance, the slurry may react in recessed regions, causing those regions to be excessively etched. Furthermore, the polishing rate of the CMP may be dependent upon the polish characteristics of the topography. As a result, the polishing pad, being somewhat conformal to the surface topography, may deform in response to polishing laterally adjacent layers comprising different polish properties. Therefore, while the removal rate of raised regions of the dielectric may be greater than that of the recessed regions, a significant amount of the recessed regions may, unfortunately, undergo removal. This phenomena is known as the "dishing" effect and may reduce the degree of planarization that can be achieved by the CMP process. Consequently, the "dishing" effect may cause upper surfaces of structures and layers to curve below polished upper surfaces of adjacent structures or layers. For example, relatively shallow trench isolation regions are typically formed within a semiconductor substrate to isolate impurity regions of active devices placed in the substrate. The dishing effect may be so severe that some portions of the upper surface of the shallow trench isolation regions may extend below the upper surface of the substrate by approximately 500 angstroms. As a result, the active regions of the device may not be adequately isolated.

To insure that the upper surfaces of isolation regions are above or coplanar with upper surfaces of adjacent active regions, a polish stop layer may be used to terminate the polishing process at an elevation above the semiconductor substrate. The composition of the polish stop layer is such that it polishes much more slowly than the layer above it. In this manner, polishing may be substantially terminated upon exposing the polish stop layer. Thus, layers or structures formed upon the semiconductor topography adjacent to the polish stop layer may also be polished to approximately the same elevation level as the polish stop layer. Silicon nitride is typically used as a polish stop layer since it is a relatively hard material, particularly compared to silicon dioxide.

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As such, a technique with which to form shallow trench isolation regions may include depositing a layer of silicon nitride ("nitride") across an upper surface of a semiconductor substrate. A "pad" oxide layer is typically interposed between the substrate and nitride layer to reduce inherent stresses between nitride and silicon.

- 5 Portions of the nitride layer and substrate are etched away to define a trench within the substrate. Fill oxide (i.e., silicon dioxide) is then deposited into the trench to a level spaced above the upper surface of the nitride layer. The resulting upper surface of the fill oxide includes a recessed region elevationally raised above the trench area. A trench isolation region may then be formed by subjecting the semiconductor topography to a
- 10 CMP process. The polish rate of the nitride layer is so slow that the nitride layer acts as a polish stop layer. Subsequent to the CMP process, the nitride layer may be removed by a nitride strip followed by a selective etch technique to remove the pad oxide.

- A disadvantage of the polish stop process described above is a problem known as
- 15 the "dishing effect". During the CMP process, the slurry, being a relatively viscous fluid, may flow to the recessed region of the fill oxide. Further, the polishing pad, being somewhat conformal to the semiconductor topography, may deform above the recessed region in response to the polishing characteristic differences between the fill oxide and nitride layer. Consequently, the fill material may be undesirably "dug out" of some
- 20 trenches and thus, the "dishing effect" may be observed. The "dishing effect" may be further augmented by "overpolishing" the polish stop layer. It is important to remove all fill oxide above the nitride layer for subsequent removal of the polish stop layer. Therefore, the surface may be "overpolished" or polished to a level spaced below the original upper surface of the nitride layer to ensure that the fill oxide no longer resides
- 25 above the nitride layer. Furthermore, the dishing effect may be dependent on pattern density. For example, a pattern having relatively few and/or relatively narrow isolation trenches may include a large amount of nitride across the lateral portion of the topography, which results in a slower polish rate. Alternatively, patterns having relatively

many and/or wide isolation trenches may include less nitride across the lateral surface of the semiconductor topography, resulting in a faster polish rate and a thicker amount of nitride needed to compensate for the increase in the polish rate.

5           It is, therefore, advantageous to form a polish stop layer having a sufficient thickness such that the "dishing effect" does not extend below the upper most surface of the substrate subsequent to polishing. Typically, the thickness of the polish stop layer may be greater than 500 angstroms and possibly greater than 1000 angstroms. Unfortunately, the use of a relatively thick polish stop layer may create a significant step  
10 height between the resulting shallow trench isolation region and adjacent regions upon removal of the polish stop layer. The "step height" as used herein refers to the upper portion of the shallow trench isolation region that extends above the upper surface of adjacent regions. Such a step height may have a thickness between approximately 500 angstroms and approximately 2000 angstroms. Unfortunately, this step height may be  
15 significant enough to cause the aforementioned problems associated with non-planar surfaces. In addition, incomplete removal of subsequently deposited polysilicon at step edges may result in the formation of "poly stringers" in subsequent processing, which may adversely affect the performance of the circuit. Furthermore, since the nitride layer increases the depth of the trench which must be filled by the fill oxide, a thicker fill oxide  
20 is needed. Such a formation of a relatively thick fill oxide above the nitride layer can be rather time-consuming and costly.

          Accordingly, it would be advantageous to develop a method for forming a semiconductor topography having a substantially planar upper surface across the entire  
25 semiconductor topography. In particular, it would advantageous to reduce the thickness of or eliminate a polish stop layer for the formation of a substantially planar surface.

## SUMMARY OF THE INVENTION

The problems outlined above may be in large part addressed by a method for processing a semiconductor topography. In particular, a method is provided in which a  
5 polish stop layer may be eliminated from a polishing process. Such a method may include polishing an upper layer of a semiconductor topography to form an upper surface at an elevation above an underlying layer, wherein the upper surface does not include a polish stop material. Preferably, the upper surface of the topography formed by polishing is spaced sufficiently above the underlying layer to avoid polishing the underlying layer.  
10 The entirety of the upper surface may be simultaneously etched to expose the underlying layer. In an embodiment, the underlying layer may comprise a lateral variation in polish characteristics. In other words, the layer may include a variation in material composition, in which the different materials polish differently. For example, the underlying layer may include a silicon substrate patterned with dielectric filled trenches. In another  
15 embodiment, the underlying layer may include silicon nitride laterally interspersed with silicon dioxide. In yet another embodiment, the underlying layer may include conductive regions laterally interspaced with dielectric regions.

In an embodiment, a method for processing a semiconductor topography may  
20 include using fixed abrasive polishing of a dielectric layer for reducing a required thickness of an additional layer underlying the dielectric layer. The dielectric layer may include an interlevel dielectric or a trench fill layer for shallow trench isolation regions. The fixed abrasive polishing process may include applying a fluid substantially free of particulate matter between the semiconductor topography and an abrasive polishing  
25 surface. The additional layer may be used, for example, as a step-definition layer. In particular, the additional layer may be used to form a layer with step heights of less than approximately 200 angstroms. In such an embodiment, the additional layer may have a reduced thickness of less than approximately 500 angstroms, or more preferably approximately 150 angstroms or less. In another embodiment, the additional layer may  
30 be completely eliminated. Furthermore, the additional layer may have different polishing

characteristics than that of the dielectric layer. For example, in an embodiment in which the dielectric layer includes silicon dioxide, the additional layer may include silicon nitride or another material which has different polishing characteristics than that of silicon dioxide. The method may further include etching the dielectric layer subsequent  
5 to polishing the dielectric layer. Such a method may be useful when exposing an underlying layer is desirable by techniques other than polishing. For example, the method herein may be particularly useful for shallow trench isolation formation or planarizing interlevel dielectric layers.

10 In an embodiment, the method for processing a semiconductor topography may include polishing an upper layer of said semiconductor topography to form a polished upper surface of the semiconductor topography at an elevation above an underlying layer that includes a lateral variation of polishing characteristics. The method may further include etching the entirety of the upper surface of the semiconductor topography  
15 simultaneously to expose the underlying layer. In this manner, the entire lateral upper surface of the semiconductor topography may be etched at one time. This is in contrast to an etch step performed after polishing down to a polish stop, since such an etch step selectively etches the polish stop portion of the upper surface and not the adjacent portions. In one embodiment, the upper layer may include an interlevel dielectric layer.  
20 The interlevel dielectric layer may include silicon dioxide, silicon nitride, silicon carbide, or carbonated polymers. Preferably, the polished upper surface of the semiconductor topography is spaced sufficiently above the underlying layer to avoid dishing during polishing. In general, the polished upper surface of the semiconductor topography may be spaced sufficiently above the underlying layer to avoid polishing the underlying layer.  
25 For example, the upper surface may be formed above the underlying layer at an elevation between approximately 100 angstroms and approximately 1000 angstroms. In one embodiment, the polishing process may include a fixed abrasive polishing process. Such a polishing process may form a substantially planar upper surface. The underlying layer



may include a silicon substrate patterned with dielectric filled trenches or silicon nitride regions laterally interspersed with silicon dioxide regions. Alternatively, the underlying layer may include conductive regions interspersed with dielectric regions.

5            Terminating the polishing process at an elevation above a patterned layer of materials, which include a variation of polishing characteristics, may prevent the occurrence of dishing of the patterned layer during the polishing process. Therefore, the polishing process may be designed to terminate at an elevation above such an underlying layer. For example, the polishing process may be programmed to polish for a  
10       predetermined period of time. In one embodiment, a substantially planar surface may not be formed upon termination of the polishing process if the thickness of overlying layers is not sufficient to form a substantially planar surface during the polishing process. In such an embodiment, the upper surface of the semiconductor topography formed by polishing may comprise materials with a variation of etch characteristics (though not a variation of  
15       polish characteristics). As such, a substantially planar surface may be obtained subsequent to the etch process. Alternatively, the overlying layers may be thick enough for the polishing process to form a substantially planar surface spaced above an underlying layer.

20           In an embodiment, the polishing rate may be significantly reduced when a substantially planar surface is formed. Such a polishing process may include a fixed abrasive polishing process, which is a polishing process in which abrasive material is fixed into the polishing pad rather than being suspended in a liquid to form a slurry. A fixed abrasive process may be achieved by modification of a CMP process. However,  
25       contrary to some CMP processes, the polishing rate of the fixed abrasive polishing process is significantly reduced upon forming a substantially planar surface. As such, a fixed abrasive polishing process may be programmed to run longer than a CMP process. Such an over polishing technique may be used to insure that a substantially planar surface has been obtained. Alternatively, the polishing process may be designed to automatically  
30       terminate upon indication of a significant reduction in the polishing rate. Consequently,

the method as described herein may be designed such that the upper surface of the semiconductor topography subsequent to polishing may be spaced sufficiently above an underlying layer to avoid polishing the underlying layer. Furthermore, the thickness of the upper layer upon deposition may be optimized to allow the polishing process to  
5 terminate on its own, and yet minimize the elevation above an underlying layer subsequent to polishing. In one embodiment, the upper surface of the semiconductor topography subsequent to polishing may be spaced above an underlying layer by an amount between approximately 100 angstroms and approximately 1000 angstroms. Preferably, the upper surface of the semiconductor topography subsequent to polishing  
10 may be approximately 500 angstroms above the underlying layer. As such, such a polishing process may eliminate the use of a polish stop layer. In this manner, the upper surface of the semiconductor topography formed subsequent to polishing may not include a polish stop material.

15 The etch process may include a single etch step or a series of etch steps. In either embodiment, the method may include an initial etch step which etches the entire lateral upper surface of the semiconductor topography at one time. In this manner, a non-selective removal of exposed material across the semiconductor topography may be conducted simultaneously. In addition to the initial etch step, other etch steps may be  
20 employed. For example, if silicon nitride is interposed between the upper surface of the semiconductor topography and an underlying layer, a separate nitride etch step may be required to remove portions of the nitride after the initial etch step. A further etch step may be needed after the nitride strip to remove other material remaining above the underlying layer. In an embodiment in which the underlying layer includes a lateral  
25 variation in polishing characteristics, the etch process allows the underlying layer to be exposed, but does not produce dishing of the underlying layer as may occur when polishing a layer including materials with different polishing characteristics.

The method as described herein may be used for the fabrication of shallow trench isolation regions. In such an embodiment, a trench fill material may be blanket deposited over a semiconductor topography comprising one or more trenches. Preferably, the entirety of the upper surface of the deposited trench fill material is spaced above the  
5 portion of the trench within the semiconductor substrate, such that an upper surface of the semiconductor topography subsequent to a polishing process may be formed at an elevation above the semiconductor substrate. Furthermore, the upper surface of the semiconductor topography subsequent to polishing preferably does not include a polish stop material. The polishing process may include a fixed abrasive polishing process as  
10 described above. The entirety of the planar surface may be simultaneously etched such that remaining portions of the trench fill material subsequent to etching are laterally confined within the trenches. The etch process may include a single etch step or a series of etch steps as discussed above.

15 Such a process may produce shallow trench isolation regions that are substantially coplanar with laterally adjacent regions. In this manner, the upper surface of the trench fill material subsequent to etching may be substantially coplanar with the upper surface of the semiconductor substrate. Alternatively, a step height may be formed between the trenches and adjacent regions during the etch process due to a variation in etch rate  
20 characteristics of layers positioned upon the underlying layer. The step height may be positive or negative depending on the etch rate properties of the materials etched. As such, the upper surface of the trench fill material subsequent to etching may be below or above the upper surface of the semiconductor topography. More specifically, the upper surface of the trench fill material subsequent to etching may be less than approximately  
25 200 angstroms above the upper surface of the semiconductor topography. Preferably, the upper surface of the trench fill material subsequent to etching may be less than approximately 50 angstroms above the upper surface of the semiconductor topography.

In an embodiment, an intermediate layer may be formed upon an upper surface of the semiconductor topography prior to depositing the trench fill material. Such an intermediate layer may help to achieve a desired step height of the trench fill material above the substrate at the end of the shallow trench isolation process. As such, the intermediate layer may be formed upon the upper surface of the semiconductor topography adjacent to the trenches. In this manner, the intermediate layer may be interposed between the underlying layer and the trench fill material in regions of the topography adjacent to the trenches. Therefore, the intermediate layer may be polished and/or etched in conjunction with the process as described herein. The intermediate layer may include, for example, a base oxide layer. In one embodiment, the intermediate layer may have a different etch rate than the trench fill material. For instance, the intermediate layer may include a doped oxide layer, such as borosilicate, borophosphosilicate glass (BPSG), phosphosilicate glass (PSG), fluorinated silicate glass, or any combination of silicon dioxide with elements from columns 3 and 5 of the periodic table. Alternatively, the intermediate layer may include a nitride layer. In such an embodiment, the thickness of the nitride layer may be less than approximately 500 angstroms. More specifically, the nitride layer may have a thickness between approximately 100 angstroms and approximately 200 angstroms. Furthermore, the intermediate layer may include either a layer of silicon carbide or carbonated polymer. Such layers, as with the doped oxide layer or nitride layer, may be arranged upon a layer of base oxide.

In an embodiment, the method for processing a semiconductor topography may include using a fixed abrasive polishing process for eliminating the use of a polish stop layer. In particular, the method may be used to polish a dielectric layer. The dielectric layer may include an interlevel dielectric or a trench fill layer for formation of shallow trench isolation regions. For instance, the method may be used to fabricate a shallow trench isolation region without the use of a polish stop layer, such that an upper surface of the isolation region may be elevationally above the upper surface of the surrounding substrate. In particular, the upper surface of the isolation region may be less than approximately 200 angstroms above the upper surface of the surrounding substrate. The

fixed abrasive polishing process may include applying a fluid substantially free of particulate matter between the semiconductor topography and an abrasive polishing surface. In an embodiment, the fixed abrasive polishing process may form a substantially planar surface at an elevation above the semiconductor substrate. In such an  
5   embodiment, the planar surface may include the trench fill material. The method may further include etching the entirety of the planar surface simultaneously after the fixed abrasive polishing process. The planar surface may include a lateral variation of materials, where the materials have different etch characteristics. In addition, the etching process may include etching an intermediate layer, which is interposed between the planar  
10   surface and the substrate. The intermediate layer may also include materials of different etch characteristics.

There may be several advantages to eliminating the use of a polish stop layer, and in some embodiments replacing it with a step-definition layer. For example, a shallow  
15   trench isolation region having a reduced step height may be formed. Such a benefit offers the formation of a substantially planar upper surface upon a semiconductor topography. In this manner, additional structures and layers may be formed within design specifications of the device. Furthermore, step coverage problems and lithography problems may be minimized. The method as described herein may also minimize pattern  
20   density constraints since the "dishing effect" is reduced. Other benefits may include a decrease in material use with a reduction in thickness of the upper layer and the elimination of the polish stop layer. Furthermore, the number of processing steps may be reduced. Such reductions and eliminations may reduce processing time, thereby increasing production throughput. Material costs and labor costs may also be reduced.

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## **BRIEF DESCRIPTION OF THE DRAWINGS**

Other objects and advantages of the invention will become apparent upon reading the following detailed description and upon reference to the accompanying drawings in  
5 which:

Fig. 1 depicts a partial cross-sectional view of a semiconductor topography in which an intermediate layer and a resist layer are formed upon a semiconductor layer;

10 Fig. 2 depicts a partial cross-sectional view of the semiconductor topography in which the resist layer is patterned subsequent to the layer formations of Fig. 1;

Fig. 3 depicts a partial cross-sectional view of the semiconductor topography in which trenches are formed within the intermediate layer and semiconductor layer  
15 subsequent to the resist layer patterning of Fig. 2;

Fig. 4 depicts a partial cross-sectional view of the semiconductor topography in which an upper layer is formed within the trenches and above the intermediate layer subsequent to the trench formation of Fig. 3;

20 Fig. 5 depicts a partial cross-sectional view of the semiconductor topography in which the upper layer is polished to an elevation above the intermediate layer subsequent to the upper layer formation of Fig. 4;

25 Fig. 6 depicts a partial cross-sectional view of the semiconductor topography in which the entire upper surface of the upper layer is etched subsequent to the upper layer polishing of Fig. 5;

Fig. 7 depicts a partial cross-sectional view of the semiconductor topography in  
30 which an upper portion of the intermediate layer is etched subsequent to the upper surface etching of Fig. 6;

Fig. 8 depicts a partial cross-sectional view of the semiconductor topography in which remaining portions of the intermediate layer are etched to form isolation regions subsequent to the upper portion etching of Fig. 5;

5        Fig. 9 depicts a partial cross-sectional view of the semiconductor topography in an alternative embodiment, in which the upper layer is polished to an elevation within an upper portion of the intermediate layer, subsequent to the upper layer formation of Fig. 4;

10       Fig. 10 depicts a partial cross-sectional view of the semiconductor topography in which remaining portions of the intermediate layer are etched to form isolation regions subsequent to the upper layer polishing of Fig. 9;

15       Fig. 11 depicts a partial cross-sectional view of the semiconductor topography in an alternative embodiment, in which the upper layer is polished to an elevation within a lower portion of the intermediate layer, subsequent to the upper layer formation of Fig. 4; and

20       Fig. 12 depicts a partial cross-sectional view of the semiconductor topography in which remaining portions of the intermediate layer are etched to form isolation regions subsequent to the upper layer of polishing Fig. 11.

25       While the invention is susceptible to various modifications and alternative forms, specific embodiments thereof are shown by way of example in the drawings and will herein be described in detail. It should be understood, however, that the drawings and detailed description thereto are not intended to limit the invention to the particular form disclosed, but on the contrary, the intention is to cover all modifications, equivalents and alternatives falling within the spirit and scope of the present invention as defined by the appended claims.

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## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Turning to the drawings, exemplary embodiments of a method for processing a semiconductor topography are shown in Figs. 1-12. In particular, a method is provided in which a polish stop layer may be eliminated from a polishing process. Fig. 1 depicts semiconductor topography 37 in which dielectric 32 may be formed upon semiconductor layer 20. Moreover, layer 34 may be formed upon dielectric 32, and resist 36 may be formed upon layer 34. Layers 32 and 34 may together form intermediate layer 33. Alternatively, intermediate layer 33 may include only either dielectric 32 or layer 34. In such an embodiment, the layer not included in intermediate layer 33 may be omitted. In particular, layer 34 may be omitted and thus resist layer 36 may be formed upon and in contact with underlying dielectric 32. Moreover, layer 34 may be formed upon and in contact with semiconductor layer 20 if dielectric 32 is omitted. In contrast, intermediate layer 33 may be omitted (omitting both layers 32 and 34) from Fig. 1, such that resist layer 34 may be formed upon and in contact with semiconductor layer 20.

Semiconductor layer 20 may be a semiconductor substrate such as a silicon substrate, and may be doped either n-type (for producing a p-channel transistor) or p-type (for an n-channel transistor). More specifically, semiconductor layer 20 may be an epitaxial silicon layer grown on a monocrystalline silicon substrate, or an n-type or p-type well region formed in a monocrystalline silicon substrate. Alternatively, semiconductor layer 20 may include structures and layers formed upon a semiconductor substrate, such as a monocrystalline silicon semiconductor substrate. The structures and layers may include, but are not limited to, gate dielectric layers, gate structures, contact structures, local interconnect wires, additional dielectric layers, or metallization layers. In this manner, semiconductor layer 20 may be substantially planar or may have substantial elevational differences due to the formation of such structures and layers. Doped regions (not shown) may also be formed in semiconductor layer 20. For example, doped regions may be lightly doped drain regions and heavily doped source/drain regions formed in a semiconductor layer adjacent to gate structures.



Dielectric 32 may serve as a "pad oxide" to reduce inherent stresses between an overlying layer and semiconductor layer 20. In another embodiment, dielectric 32 may also promote adhesion of an overlying layer upon semiconductor layer 20. Dielectric 32  
5 may be grown upon semiconductor layer 20 using wet or dry thermal oxidation of a silicon substrate. Alternatively, dielectric 32 may be deposited on semiconductor layer 20 using chemical-vapor deposition ("CVD") from, for example, a gas that may include  $\text{SiH}_4$  and  $\text{O}_2$ . Typically, thermally grown oxides etch at a slower rate than deposited oxides. Therefore, the selection of the oxide formation technique may depend on the etch  
10 characteristics needed in the subsequent etching process. Dielectric 32 may have a thickness, for example, between approximately 50 angstroms to approximately 250 angstroms. Dielectric 32 may include a dielectric material, such as silicon dioxide ( $\text{SiO}_2$ ), silicon oxynitride ( $\text{SiO}_x\text{N}_y(\text{H}_z)$ ), or silicon dioxide/silicon nitride/silicon dioxide (ONO).

15 Layer 34 may serve to protect portions of underlying layers and structures within semiconductor layer 20. For example, layer 34 may protect portions of dielectric 32 and semiconductor layer 20 from an etch process which may be used to form trenches within semiconductor layer 20. Alternatively or in addition, layer 34 may serve as a step-definition layer. In this manner, layer 34 may be used to subsequently form a layer  
20 including step heights. In a preferred embodiment, the step heights may be less than approximately 200 angstroms. As such, layer 34 may have, for example, a thickness of approximately 50 angstroms to approximately 500 angstroms and preferably approximately 150 angstroms. Appropriate materials for layer 34 may include any material having a substantially different etch rate than upper layer 42. In particular, layer  
25 34 may comprise a material having a lower etch rate than that of upper layer 42 discussed in the description of Fig. 4 below. On the other hand, layer 34 may be a doped dielectric layer, which may have a higher etch rate than that of upper layer 42. In particular, layer 34 may include any combination of silicon dioxide with elements from columns 3 and 5 of the periodic table. For example, layer 34 may include borophosphorus silicate glass  
30 (BPSG) or phosphorus silicate glass (PSG). In an embodiment, BPSG may have a boron

concentration of less than approximately 5% by weight. PSG may have a phosphorus concentration of less than approximately 10% by weight, and more preferably less than approximately 5% by weight. In other embodiments, layer 34 may include either silicon carbide or carbonated polymer. Alternatively or in addition, layer 34 may include a material having different polishing characteristics than that of upper layer 42 of Fig. 4. For instance, layer 34 may include silicon nitride deposited by thermally decomposing silane and ammonium in a chemical vapor deposition process maintained at a temperature in the range of approximately 200°C to approximately 800°C.

10 In an embodiment, resist 36 may be formed upon layer 34. Resist 36 may include a photoresist, such as a deep ultraviolet resist, an I-line resist, a G-line resist, or another resist, such as an e-beam resist or an x-ray resist. Resist 36 may be patterned using a lithography technique, thus exposing portions 38 of layer 34 as shown in Fig. 2. Exposed portions 38 of layer 34 and underlying portions of dielectric 32 and semiconductor layer 20 may be etched to form trenches 40 as shown in Fig. 3. The etch process may include wet etch and/or dry etch techniques. The patterned photoresist may then be removed by a stripping process such as a wet etch or a reactive ion etch stripping process. Trenches 40 may be used to subsequently form shallow trench isolation regions within semiconductor layer 20. Isolation regions may be field oxide regions, which may serve to isolate separate active regions on semiconductor layer 20 from one another.

Turning to Fig. 4, trenches 40 may be filled with upper layer 42. Upper layer 42 may also be formed upon layer 34, which may be formed adjacent to trenches 40. Alternatively, upper layer 42 may be formed upon and in contact with dielectric 32 if layer 34 is omitted from the embodiment. In another embodiment, upper layer 42 may be formed upon and in contact with semiconductor layer 20 if intermediate layer 33 is omitted. Upper layer 42 may include a material including different polishing characteristics than that of semiconductor layer 20. For example, upper layer 42 may include a polycrystalline dielectric layer or an amorphous dielectric layer. Thus, upper layer 42 may include silicon dioxide ( $\text{SiO}_2$ ), silicon nitride ( $\text{Si}_x\text{N}_y$ ), silicon oxynitride ( $\text{SiO}_x\text{N}_y$ )

(H<sub>2</sub>)), silicon dioxide/silicon nitride/silicon dioxide (ONO), silicon carbide, or carbonated polymers. Alternatively, upper layer 42 may be formed from a low-permittivity ("low-k") dielectric, generally known in the art as a dielectric having a dielectric constant of less than about 3.5. One low-k dielectric in current use, which is believed to make a  
5 conformal film, is fluorine-doped silicon dioxide. Upper layer 42 may also be undoped or may be doped to form, for example, low doped borophosphorus silicate glass (BPSG), low doped phosphorus silicate glass (PSG), or fluorinated silicate glass (FSG). Low doped BPSG may have a boron concentration of less than approximately 5% by weight. Low doped PSG may have a phosphorus concentration of less than approximately 10% by  
10 weight, and more preferably less than approximately 5% by weight.

In an embodiment in which upper layer 42 includes different polishing characteristics than that of semiconductor 20, an underlying layer including a variation of polishing characteristics may be formed. The patterned underlying layer may be defined  
15 as the portion of semiconductor topography 37 comprising laterally adjacent materials of varied polishing characteristics. For example, the patterned underlying layer 41 may be the portion of semiconductor topography 37 comprising semiconductor layer 20 and laterally adjacent regions of upper layer 42. In this manner, upper layer 42 may comprise silicon dioxide and semiconductor layer 20 may comprise silicon. Alternatively,  
20 patterned underlying layer 43 may be the portion of semiconductor topography 37 comprising layer 34 and laterally adjacent regions of upper layer 42, when layer 34 comprises silicon nitride and upper layer 42 includes a dielectric such as oxide.

Furthermore, upper layer 42 may be deposited conformally and thus, may have a  
25 non-planar upper surface as shown in Fig. 4. Alternatively, upper layer 42 may be relatively planar if the underlying structures and layers are substantially planar before the deposition of upper layer 42. Preferably, upper layer 42 may be formed upon semiconductor topography 37 of Fig. 4 such that the entirety of the upper surface of upper layer 42 is spaced above semiconductor 20. Forming upper layer 42 to such a thickness  
30 allows semiconductor topography 37 to be subsequently polished to a substantially planar

surface spaced above semiconductor layer 20. In one embodiment, upper layer 42 may be formed to such a thickness that the entirety of the upper surface of upper layer 42 may be spaced above trenches 40. Trenches 40 refer to the depressions formed within the semiconductor topography 37 by the etch process of Fig. 3. Consequently, the height of the trenches may depend upon the layers present during the etch process. As such, Fig. 4 illustrates the entirety of the upper surface of upper layer 42 above the upper surface of layer 34. However, upper layer 42 may be deposited in a manner such that the entirety of its upper surface may be above the upper surface of semiconductor layer 20, but below the upper surface of intermediate layer 33. Such an embodiment may be particularly beneficial when layer 34 includes a material comprising a higher etch rate characteristic than that of upper layer 42, i.e., doped oxide material. The faster etch rate of the doped oxide as compared to upper layer 42 may subsequently form isolation regions essentially co-planar with semiconductor layer 20. Alternatively, isolation regions with positive step heights may result due to the difference in etch rate characteristics.

Subsequent to Fig. 4, semiconductor topography 37 may be polished to an elevation above semiconductor layer 20 to prevent polishing underlying layer 41 or 43. As such, the polishing process may be designed to terminate at an elevation above semiconductor layer 20 to prevent the occurrence of dishing of subsequently formed shallow isolation trench regions. Damage to the silicon surrounding the isolation regions may also be prevented. In one embodiment, the polishing process may be programmed to polish for a predetermined period of time. In such an embodiment, a substantially planar surface may not be formed upon termination of the polishing process if the upper surface of upper layer 42 is not sufficiently above trenches 40 prior to polishing. Alternatively, upper layer 42 may be thick enough for the polishing process to form a substantially planar surface spaced above underlying layer 41 or 43. A layer sufficiently above an underlying layer may be defined as a layer thick enough in which a substantially planar surface may be formed within the layer during a polishing process. The planarity of a surface may be defined by the elevational variation of the upper surface across the entirety of semiconductor topography 37 with respect to an underlying plane within the

topography. In an embodiment, a substantially planar surface may be defined as an upper surface with an elevational variation of approximately 200 angstroms or less across the entirety of the semiconductor topography.

5 In a preferred embodiment, the polishing process may significantly reduce its polishing rate above an underlying layer of varying polishing characteristics. Such a reduction in the polishing rate may be accomplished through the use of a fixed abrasive polishing process. The fixed abrasive polishing process may reduce its polishing rate upon forming a substantially planar surface. As such, a fixed abrasive polishing process  
10 may be programmed to run longer than a CMP process. Such an over polishing technique may be used to insure that a substantially planar surface has been obtained. Alternatively, the polishing process may be designed to automatically terminate upon indication of a significant reduction in the polishing rate. In an embodiment, this may be accomplished through flatness detection of the semiconductor topography during the  
15 polishing process. Such detection may include, for example, monitoring the current drawn by the motor or the concentration of the effluent. These detection methods may also be used to pre-calibrate timed processes. Consequently, the method as described herein may be designed such that the upper surface of upper layer 42 subsequent to polishing may be spaced sufficiently above underlying layer 41 or 43 to avoid polishing  
20 the underlying layer and thereby preventing dishing of the underlying layer. Furthermore, the thickness of upper layer 42 may be optimized to allow the polishing process to terminate on its own, and yet minimize the elevation of the polished underlying layer 41 or 43. In one embodiment, the upper surface of semiconductor topography 37 subsequent to polishing may be spaced above an underlying layer by an amount between  
25 approximately 100 angstroms and approximately 1000 angstroms. Thicknesses lower than this range may be undesirably thin, since it may be difficult to control the polishing process to this thickness consistently. Thicknesses larger than this range may be undesirably thick, since more material will have to be subsequently etched. In a preferred embodiment, the upper surface of semiconductor topography 37 subsequent to polishing  
30 may be approximately 500 angstroms above an underlying layer.

To avoid the problems associated with conventional CMP processes, a fixed abrasive polishing process may be employed to polish semiconductor topography 37 in the method as described herein. The fixed abrasive process involves placing a fluid, which is substantially free of particulate matter between the surface of the topography and an abrasive polishing surface of a rotating polishing pad. Alternatively, the process may be substantially free of fluid completely. The polishing surface may include a polymer-based matrix entrained with particles selected from the group consisting of cerium oxide, cerium dioxide, aluminum oxide, silicon dioxide, titanium oxide, chromium oxide, and zirconium oxide. The fluid applied to the polishing surface in a fixed abrasive process may include deionized water or a reactive fluid such as a base diluted with water, depending upon the features of the topography being polished. The fluid may be used to wash away contaminants resulting from the polishing process. However, a fluid comprising a reactive substance may limit the ability of the process to significantly reduce the polishing rate upon forming a substantially planar surface.

An etching process may follow the polishing process by etching the entirety of the upper surface of the topography simultaneously to expose semiconductor layer 20 and laterally adjacent isolation regions. In this manner, the etch process allows semiconductor layer 20 to be exposed, but does not produce dishing of isolation regions. Etch methods may include the use of wet etch chemistries or dry etch techniques. As discussed below, the etch process may include a single etch step or a series of etch steps. In either embodiment, the method may include an initial etch step which etches the entire lateral upper surface of semiconductor topography 37 at one time. The initial etch step may include, for example, subjecting semiconductor topography 37 to an etch chemistry comprising hydrofluoric acid. In this manner, a non-selective removal of exposed oxide material may be conducted. Alternatively, other etch chemistries known to those in the art may be used.

Figs. 5-12 illustrate exemplary embodiments of the method as described herein subsequent to the deposition of upper layer 42 in Fig. 4. The embodiments illustrate polishing upper layer 42 to different elevations above trenches 40 followed by an etch process to form shallow trench isolation regions. For example, the embodiment of Fig. 5 illustrates a polishing process terminating at an elevation above intermediate layer 33, particularly above underlying layer 43. This embodiment may be particularly useful when layer 34 comprises a material of significantly different polishing characteristics than that of upper layer 42, e.g., silicon nitride when layer 42 is oxide. Since polishing such a material may undesirably cause dishing of the regions of upper layer 42 laterally adjacent to such a material, the polishing process preferably terminates at an elevation above underlying layer 43 when layer 34 comprises such a material. In this manner, when layer 34 comprises silicon nitride, it is not a polish stop layer, but rather a portion of an underlying layer comprising a variation of polishing characteristics. Such a layer may be useful in establishing a desired step height for a completed shallow trench isolation structure. Alternatively, layer 34 may include any of the materials discussed in Fig. 1. In either embodiment, the upper surface of the topography does not include a polish stop material subsequent to polishing.

As illustrated in Fig. 6, the entirety of upper layer 42 residing above layer 34 may be etched simultaneously. The simultaneous etch process may etch through a portion or the entirety of intermediate layer 33 in addition to etching through the entirety of upper layer 42 residing above the upper surface of layer 34. However, in an embodiment in which upper layer 34 comprises silicon nitride, the simultaneous etch process preferably terminates upon the upper surface of layer 34. In such an embodiment, a subsequent etch process selective to layer 34 may be employed as illustrated in Fig. 7. In such an etch process, layer 34 may be etched at a substantially faster rate than laterally adjacent portions of upper layer 42. As such, the upper surface of upper layer 42 may be above the upper surface of layer 32. A third etch step may then be employed in Fig. 8 to etch layer 32 and upper layer 42 simultaneously, such that isolation regions 44 may be formed. In particular, the remaining portions of upper layer 42 may be laterally confined within

trenches 40. The 3-step etch process of Figs. 6-8 may form step height 46, which is the portion of isolation regions 44 residing above semiconductor layer 20. Preferably, the upper surface of the remaining portion of upper layer 42 may be less than approximately 200 angstroms above the top of trenches 40. In one embodiment, the upper surface of the remaining portions of upper layer 42 may be less than approximately 50 angstroms above the top of trenches 40. Such step heights of minimal thickness formed above semiconductor 20 may offer the additional benefit of preventing poly stringers from forming during subsequent processing, while insuring that the active regions of the semiconductor topography are sufficiently isolated.

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In an alternative embodiment, the polishing process may be designed to terminate at an elevation within intermediate layer 33. As such, the polishing process may terminate above or within intermediate layer 33, including above or within dielectric 32 and/or layer 34. In this manner, the polishing of underlying layer 42 may be substantially terminated upon exposing layer 34 or dielectric 32. Consequently, structures or layers formed upon semiconductor layer 20 laterally adjacent to intermediate layer 33 may also be polished to approximately the same elevation level as intermediate layer 33. In this manner, intermediate layer 33 may serve as an additional layer upon which the polishing process may terminate above or within. Fig. 9 illustrates a polishing process, which polishes upper layer 42 to an elevation within layer 34. In such an embodiment, layer 34 may include any material with similar polishing characteristics to those of upper layer 42. For example, layer 34 may include a layer of doped silicon. In such an embodiment, layer 34 may be etched at a faster rate than lateral portions of upper layer 42. Fig. 10 illustrates such an etch process, thereby etching layer 34, underlying 32, and laterally adjacent regions of upper layer 42 to form isolation regions 48. As shown in Fig. 10, step height 50 may be formed due to the different etch characteristics of layer 34 and upper layer 42. The thickness of step height 50 may depend on the thickness of layer 34 and 32 in Fig. 14. As with step height 46 of Fig. 8, step height 50 is preferably less than the upper surface of the remaining portions of upper layer 42 may be less than approximately

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50 angstroms above the top of trenches 40. Alternatively, the upper surface isolation regions 48 may be substantially coplanar with the upper surface of semiconductor layer 20 or below the upper surface of semiconductor layer 20 (not shown).

5           Fig. 11 illustrates a polishing process which polishes upper layer 42 subsequent to Fig. 4 to an elevation within layer 32. In such an embodiment, the polishing process may polish through layer 34 or alternatively, layer 34 may have been omitted from the formation of the topography. The entirety of the polished upper surface may then be etched as illustrated in Fig. 12 to form isolation regions 52. In an embodiment in which  
10   layer 32 comprises a grown oxide, layer 32 may etch at slightly slower rate than the deposited dielectric material of upper layer 42. As such, a negative step height may result as shown in Fig. 12. More specifically, the upper surface of upper layer 42 may be below  
15   the upper surface of semiconductor layer 20. However, step height 50 may be minimal such that laterally adjacent active devices may still be sufficiently isolated. Preferably, the upper surfaces of isolation regions 52 may be less than 200 angstroms below the  
20   upper surface of semiconductor layer 20. In one embodiment, the upper surfaces of isolation regions 52 may be less than 50 angstroms below the upper surface of semiconductor layer 20. Alternatively, the upper surfaces of isolation regions 52 may be substantially coplanar with the upper surface of semiconductor layer 20 (not shown).

20           Although discussed above with reference to shallow trench isolation, the methods described herein may be useful in other applications involving polishing of dielectrics. In particular, methods described herein are believed to be useful for cases in which a dielectric to be polished is arranged above a layer having a lateral variation in polishing  
25   characteristics, and exposure of this layer is desired. Termination of polishing above the layer and exposure of the layer by etching may prevent undesirable effects such as polish damage or dishing. This type of application may arise, for example, during polishing of gap-fill dielectrics used between, e.g., transistor gates or interconnect lines, or between features in micro-electro-mechanical system (MEMS) structures. The methods described  
30   herein may therefore allow elimination of polish stop layers for applications other than

the shallow trench isolation embodiments described above. In cases for which an additional layer beneath a dielectric to be polished is used both as a polish stop and for other purposes (such as an etch stop, or a layer to establish a subsequent step height), removal of the need for a polish stop may allow a reduction in thickness for such an additional layer.

It will be appreciated to those skilled in the art having the benefit of this disclosure that this invention is believed to provide a method and a system for processing a semiconductor topography. Further modifications and alternative embodiments of various aspects of the invention will be apparent to those skilled in the art in view of this description. For example, the methods described herein could be applied not just to polishing a layer formed upon a semiconductor layer, but to polishing various features or layers occurring in semiconductor fabrication. It is intended that the following claims be interpreted to embrace all such modifications and changes and, accordingly, the drawings and the specification are to be regarded in an illustrative rather than a restrictive sense.